DESIGNING A 25-KILOWATT HIGH FREQUENCY SERIES RESONANT DC/DC CONVERTER

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This work was sponsored by

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Abstract

The feasibility of processing 25-kW of power with a single, transistorized, 20 kHz, series resonant converter stage has been demonstrated by the successful design, development, fabrication, and testing of such a device. It employs four Westinghouse D7ST transistors in a full-bridge configuration and operates from a 250-to-350-Vdc input bus. The unit has an overall worst-case efficiency of 93.5% at its full rated output of 1000 V and 25 A dc. A solid-state dc input circuit breaker and output-transient-current limiters are included in and integrated into the design. Circuit details of the converter are presented along with test data.

1. INTRODUCTION

To meet the goals of multi-hundred-kilowatt space power systems planned for the middle to late 1980s and beyond, advanced power-processing technology is required to convert the power available from solar arrays or other space-borne power sources to the various voltage and/or current levels required by the spacecraft bus and/or loads. This technology can be built on the strong technical base of multi-kilowatt series resonant converters [1,2,3] which have been developed in recent years. This technical base includes advanced switching components, [4] magnetic components, filter components, mathematical circuit models, [5,6] control philsophies, and switch drive strategies. [2] Much of the recent effort has been centered around the application of high power transistors in resonant converters. [2] Transistor switches display marked advantages over the more commonly applied thyristors. Among these advantages are: higher frequency operation, lower switch losses, positive commutation, lower peak tank currents, and inherent current limiting in the switch. It is anticipated that the eventual application of this technology base to multi-kilo-watt space power systems will result in both reduced specific mass due to the higher conversion frequencies, and in reduced thermal control due to more efficient operation.

To date, the highest known power level of a resonant power converter designed for space operation is 2.5 kW. [3] However, studies have shown that a module size of 25 kW is appropriate for a multi-hundred-kilowatt space-power system. A 10-kW transistorized dc/dc resonant power converter [2] designed for laboratory testing was developed by Hughes for NASA's Lewis Research Center. This contractual program was established to take the development of series resonant converters to the 25-kW power level for spaceborne and airborne applications.

The goals of this program were to develop a transistorized single-stage 25-kW dc/dc resonant power converter, with a minimum efficiency requirement of 92% and a maximum goal of 96%, and a resonant frequency of 20 kHz.

2. SRI OPERATING PRINCIPLES

A full-bridge series resonant inverter (SRI) is shown in Figure 1. If it is assumed that the

impedance of the output capacitor (C_O) reflected at the primary of the output transformer (T) is much less than the impedance of the series resonant capacitor (C), then the output voltage reflects into the series resonant tank as a dc voltage (V_{OR}). The polarity of V_{OR} will be positive for positive current flow in the tank circuit (L, C, and T), as shown in Figure 1, and negative for negative current flow in the tank circuit, as shown in Figure 2.

The current (i) during the time that Q_1 and Q_4 are conducting (Figures 1 and 3) will be:

$$i(t_0 \leq t \leq t_1) = \sqrt{\frac{C}{L}}\left[V_S - V_C(t_0) - V_{OR}\right] \sin \omega t + i(t_0) \cos \omega t, \quad (1)$$

where V_S is the source voltage, $V_C(t_0)$ is the voltage on capacitor C at $t = t_0$, V_{OR} is the reflected output voltage, $I(t_0)$ is the current in the tank circuit at $t = t_0$, and ω is the resonant frequency.

At $t = t_1$, any excess energy in the tank will be returned to the source through diodes D_1 and D_4 (Figures 2 and 3). At this time, the current will be

$$i(t_1 \leq t \leq t_2) = \sqrt{\frac{C}{L}}\left[V_S - V_C(t_1) + V_{OR}\right] \sin \omega t. \quad (2)$$

During this time interval, V_{OR} is negative, and the current in the tank circuit at $t = t_1$ is zero. For steady-state operating conditions, the current during time interval $t_2 \leq t \leq t_3$ (Figure 3) is

$$i(t_2 \leq t \leq t_3) = -i(t_0 \leq t \leq t_1) \quad . \quad (3)$$

The current during the time interval $t_3 \leq t \leq t_4$ is

$$i(t_3 \leq t \leq t_4) = -i(t_1 \leq t \leq t_2) \quad (4)$$

and

$$i(t_4 \leq t \leq t_5) = i(t_0 \leq t \leq t_1) \quad . \quad (5)$$

The voltage across the capacitor C will be

$$V_C = \frac{1}{C} \int i \, dt \, , \quad (6)$$

and is shown in Figure 3. Equation (1) shows that the current waveform in the switch is a half-sine wave pulse, with an initial step-rise in current on the leading edge of $i(t_0)$ (the current flowing in the commutating diode at the time the transistor is turned on). This sine-wave current is the major advantage of series-resonant inverters as compared to squarewave inverters, since it permits the switch to turn on at lower currents and off under zero-current conditions, thereby reducing the stresses and switching losses in these switches.

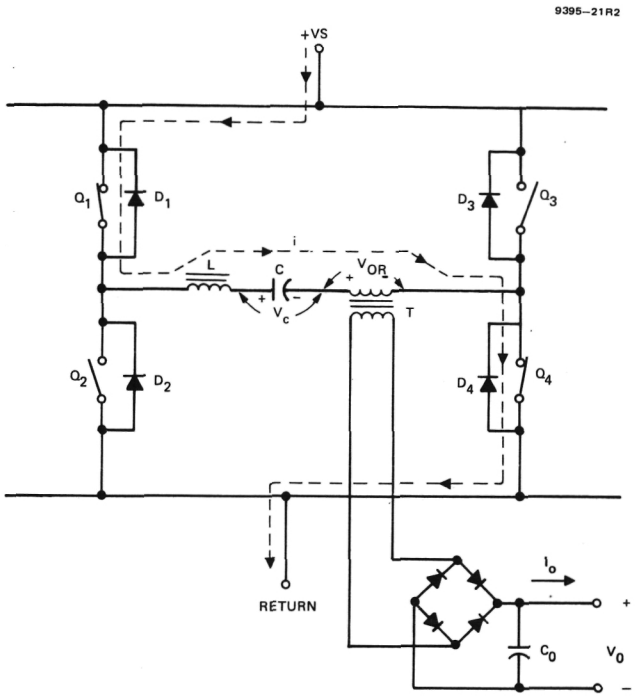

Figure 1. Current flow (i) in the SRI during the time Q_1 and Q_4 are conducting.

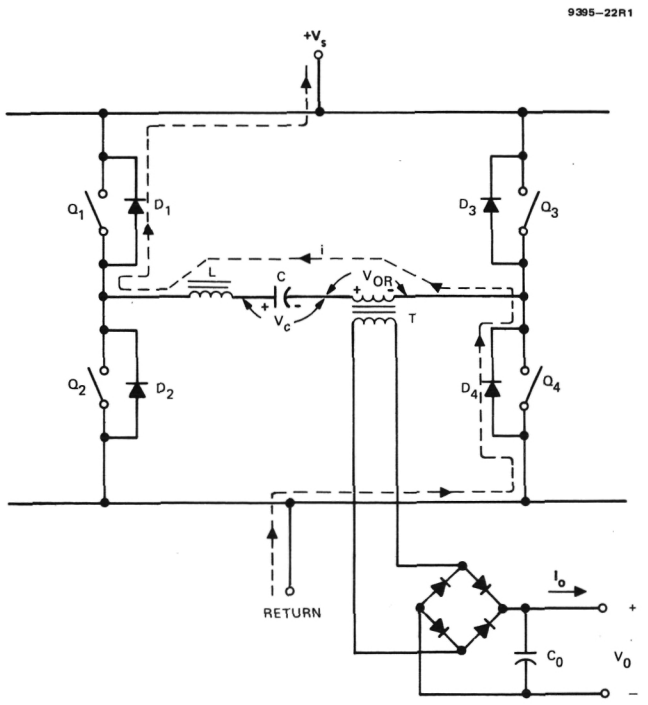

Figure 2. Current flow (i) in the SRI during the time D_1 and D_4 are conducting.

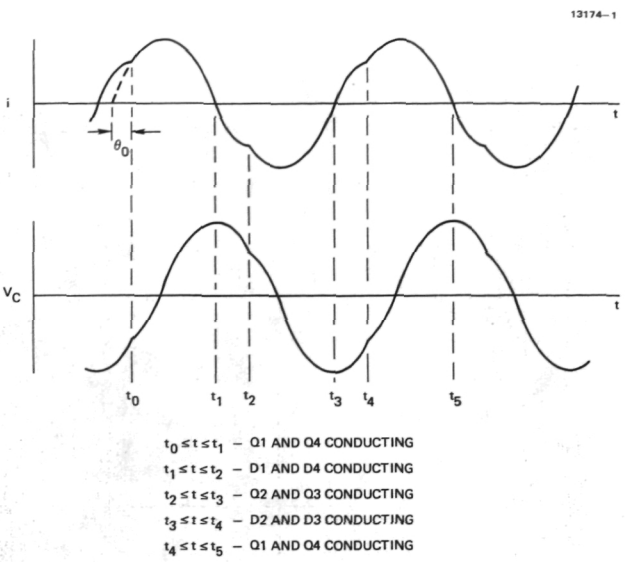

Figure 3. Tank current and resonant capacitor voltage waveforms for the circuit of Figure 1.

The output power of the inverter is $V_o \times I_o$ (see Figure 1), where V_o reflects back to the primary of the transformer T by the turns ratio, N_P/N_S. Thus,

$$V_{OR} = \frac{N_P}{N_S} V_O \quad , \tag{7}$$

where V_{OR} is the reflected voltage. V_{OR} must be less than source voltage, V_S, if series-resonant action is to occur; a value of $V_{OR} = 0.95\ V_S$ is chosen to allow for some margin in the design and still utilize most of the source voltage. Then,

$$\frac{N_S}{N_P} = \frac{V_O}{0.95\ V_S} \quad , \tag{8}$$

where V_O is the maximum output voltage desired, and V_S is the lowest operating source voltage.

With the turns ratio of the transformer defined, the average current in the primary of the transformer (which is also the average current in the tank circuit) is

$$I_{avg} = \frac{N_S}{N_P} I_O = \frac{V_O \times I_O}{0.95\ V_S} = \frac{P_o}{0.95\ V_S} \quad . \tag{9}$$

If the tank current is a pure sine wave (100 % duty cycle), then $I_{avg} = 0.637\ i_p$, where i_p is the peak value of the sine wave current.

Since the inverter cannot operate at 100% duty cycle because of the turn-on and turn-off times of the switches, the tank current cannot be a pure sine wave, and the peak tank current will have to be higher. How much higher will depend on the turn-on and turn-off times of the switches, and also on the operating frequency; however, 20% is a reasonable assumption.

The choice of L and C determines the resonant frequency of the series-resonant tank and also affects the peak current in the tank. The resonant frequency for a tank circuit is

$$f = \frac{1}{2\pi \sqrt{LC}} \quad . \tag{10}$$

Once the resonant frequency of operation has been chosen, this equation relates C to L as

$$C = \frac{1}{(2\pi f)^2 L} = \frac{1}{\omega^2 L} \quad . \tag{11}$$

The leakage inductance of the output transformer (T) in Figure 1 must be added to the inductance of the inductor (L) to obtain an equivalent inductance (L_E) for the circuit. Equation (1) can be written as

$$i = \sqrt{\frac{C}{L}}\, A \sin \omega t + \sqrt{\frac{C}{L}}\, B \cos \omega t \quad , \tag{12}$$

where

$$A = \left(V_S - V_C(t_0) - V_{OR}\right) \quad , \tag{13}$$

$$B = -\left[V_S - V_C(t_1) + V_{OR}\right] \sin \omega(t_2 - t_1) \quad , \tag{14}$$

and

$$i = \sqrt{\frac{C}{L}}\, (A \sin \omega t + B \cos \omega t) \quad . \tag{15}$$

It can be seen that i (the current in the tank circuit) is directly proportional to $\sqrt{C/L}$, where L is again L_E. Since $\sqrt{C/L} = \omega C$, it can be seen that it is also directly proportional to C. Therefore, C is chosen to provide a peak tank current large enough to produce the desired output power. Excess current in the tank contributes to losses and is therefore undesirable.

SRIs are controlled by modulating the repetition rate (frequency modulation) at which the switches in the bridge circuit are commanded to turn-on. Each command results in a half-sinusoid current pulse of the resonant tank at its natural frequency. The repetition rate varies from near zero for open-circuit-output conditions to approximately 85% of the resonant frequency (determined by the turn-on and turn-off time of the switch being employed) under full-load conditions. The parameter that is actually controlled in this manner is the average current in the tank circuit. Figure 4 shows how the normalized average tank current varies as a function of the ratio of the modulation frequency to the resonant frequency (f_m/f_r). Curves are shown for two values of q where $q = V_{OR}/V_S$. Figure 4 was normalized to unity for $q = 0.95$ and $f_m/f_r = 0.5$.

As can be seen from this figure, the average tank current increases sharply as f_m/f_r approaches unity. Thus, for lower values of q the sharp increase occurs at lower values of f_m/f_r; therefore, if the inverter is operating at a high power level and q suddenly drops due to a change in the load or an output short circuit, the control circuit must immediately lower the f_m/f_r ratio in order to prevent the peak tank current

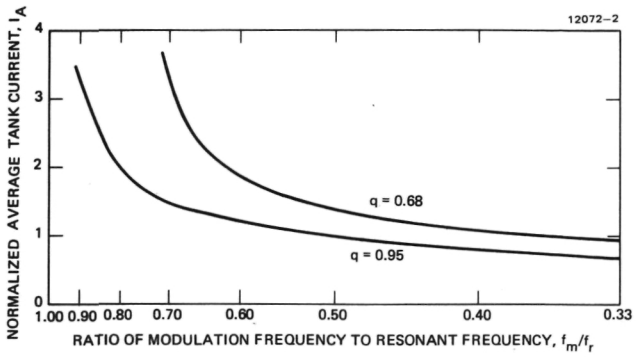

Figure 4. Normalized average tank current versus the ratio of modulation frequency to resonant frequency.

and resonant capacitor voltage from rising to destructive levels. The control circuit must also keep the time periods balanced from turning on one set of switches in the bridge to turning on the next set of switches (approximately square-wave) in order to keep the power balanced between each set of switches. If the times are not balanced, one set of switches can carry most of the power and be overstressed. The control circuit must also guarantee that the set of switches on one side of the bridge (say Q1 and Q4) are turned off before the set of switches on the other side of the bridge (Q2 and Q3) are turned on. If both sets are allowed to be on at the same time, a fault (shorted condition) will develop across the power source.

The control technique that Hughes has found to be optimal for control of SRIs is the use of a voltage-controlled-oscillator (VCO) or voltage-to-frequency converter (V/F). Under steady-state conditions, this control technique turns the switches in opposite sides of the bridge ON and OFF using a square-wave signal. The use of a square-wave signal guarantees that each side of the bridge is ON for the same amount of time, keeping the current in the tank, the current in all of the transistor switches, the voltage across the series resonant capacitor, and the flux in the transformer balanced from one half-cycle to the next. This technique results in a simpler and much more stable system than the control technique used in References 1 and 3 where the time to turn ON the other side of the bridge is determined on a half-cycle basis.

3. CONVERTER DESIGN AND DEVELOPMENT

The hardware designed, developed, fabricated, and tested under this contractual effort is shown in Figure 5. It has the following specifications and features:

- Resonant frequency - 20.6 kHz
- Input power - 250 to 350 Vdc

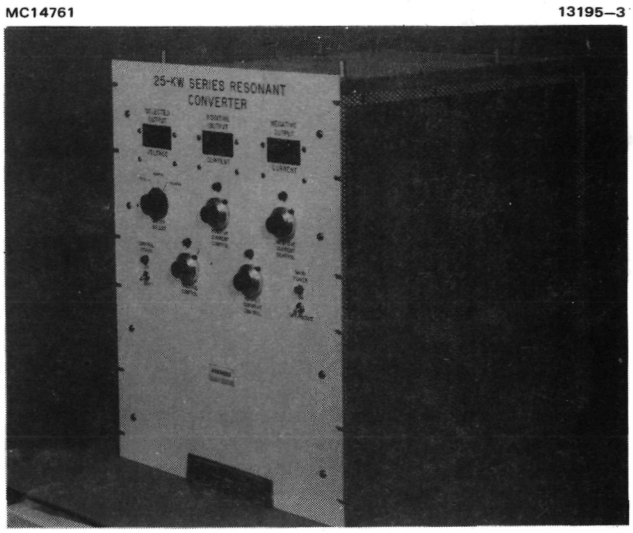

Figure 5. The 25-kW series-resonant converter.

- Output power - ±100 to ±500 V at 25 Adc or 200 to 1000 V at 25 Adc (0 to 25 kW)
- Voltage regulated - 0.1% (5% load to 100% load), output peaks a maximum of 81 V under open circuit conditions
- Current regulated - 1% (0 to 30 A)
- Output ripple - 2.5% peak to peak (200 V, 25 A), 0.9% peak to peak (1000 V, 25 A), 1.4% peak to peak (1000 V, 0 A)
- Efficiency - 94.4% (250 V input), 94.0% (300 V input), 94.0% (350 V input)
- D7ST transistor switches
- Single series-resonant power stage
- 30-kW solid-state input circuit breaker
- Transient output-current limiters
- Converter will process 30-kW at 300 V input (1000 V, 30 A output)
- Size - 48.3-cm W x 62.2cm-H x 61-cm D (19-in. W x 24.5-in. H x 24-in. D)
- Weight - 135.6 kg (299 lbs)
- Component weight - 54.3 kg (119.7 lbs) (includes harness, PC cards, and mounting hardware)
- Specific component weight - 2.17 kg/kW

The major features of the 25-kW converter design are discussed in the following sections. Further details of the design are available in Reference 7.

3.1 BRIDGE AND TANK CIRCUITRY

A schematic of the bridge and tank circuitry is shown in Figure 6. Transistors Q1 through Q4 are the four switches of the full-bridge, and T3-1 through T3-4 provide the regenerative-feed-back base-drive for these transistors. SR1 and SR2 are saturable reactors that limit the value of di/dt in Q1 through Q4, allowing these transistors to saturate quickly, thereby reducing switching losses. SR1 and SR2 saturate in approximately 500 nsec, after which they are effectively out of the circuit. Diodes CR1 through CR4 provide the paths for returning excess energy in the tank circuit to the source (commutating diodes). C3, C4, C98-X, CR33-X, CR54-X, and CR55-X suppress voltage spikes across the collectors-to-emitters of Q1 through Q4 caused by stray wiring inductance and the saturated inductance of SR1 and SR2. T5 prevents premature conduction of the commutating diodes and the associated "tailing" on the collector currents.

The series resonant tank is composed of C1, L1, and T1. The final parameter values for this tank circuit are:

- $C = 3.356\ \mu F$ (measured at 1 kHz)
- $\omega = 1.29 \times 10^5$ (20.6 kHz) (measured at 25 kW)
- $L = 17.8\ \mu H$
- $Z_0 = \sqrt{\frac{L}{C}} = 0.434\ \Omega$

Major aspects of the bridge and tank design are expanded upon below.

3.1.1 Transistor Switches

The switches used for the bridge circuit are Westinghouse D7ST transistors which have a $V_{CEO}(sus)$ rating of 500 V, a peak collector current rating of 500 A, and a power rating of 1250 W. These transistors were tested for their turn-on characteristics, saturation voltage, and storage time. Figure 7 shows the waveforms for a typical transistor. In Figure 7(a) there is a delay of approximately 100 ns from the time that the base voltage goes positive until the collector voltage starts to fall; the collector voltage then falls to 20 V in approximately 65 ns and stays in a quasi-saturation state for 350 ns before going to zero. The quasi-saturation state is very lossy and can drop the overall efficiency by 1 to 2% or more. The quasi-saturation state is caused by the rise in collector current before the base current has risen to a level sufficient to saturate the transistor (linear operation). The saturable reactors, SR1 and SR2 of Figure 6, prevent this quasi-saturation condition by delaying the rise in collector current until the base current has had a chance to get the transistor into saturation. Figure 7(b) shows a saturation voltage of approximately 0.5 V at the time of peak collector current (80 A) and a storage time of 6 μs. The measured collector voltage goes negative while the collector current is still positive because of the internal inductance of the transistor package.

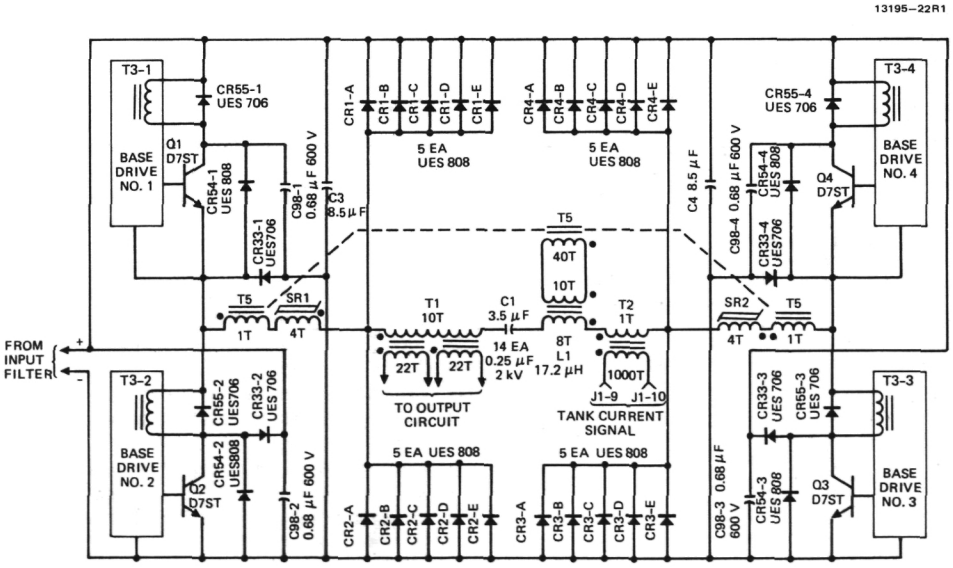

Figure 6. 25-kW series-resonant-converter bridge and tank circuitry.

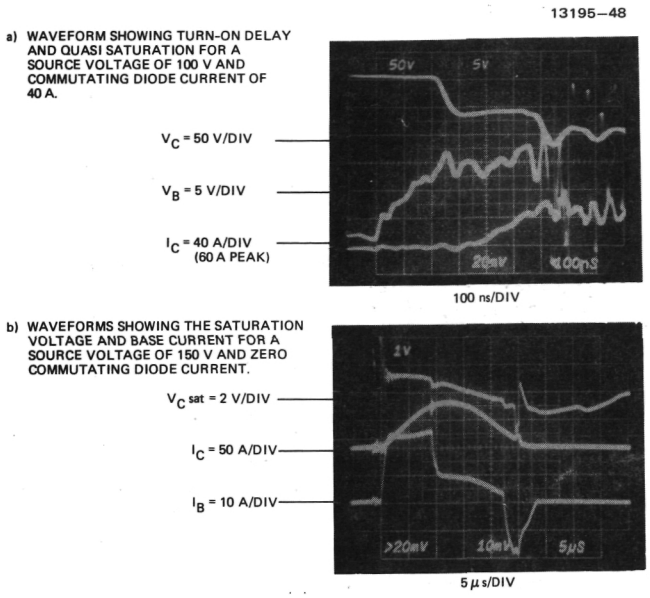

Figure 7. Typical current and voltage waveforms during testing of the D7ST transistor (transistor number 11).

3.1.2 Suppression of Voltage Spikes

Stray wiring inductance, leakage inductance of transformers, and the saturated inductance of a saturable reactor can all cause large voltage spikes (> 200 V) to occur in the circuit of Figure 6. At a bus voltage of 350 V, a 200-V spike will exceed the collector-to-emitter rating of the D7ST transistors and possibly cause the device to fail.

The diodes and capacitors used for voltage spike suppression in Figure 6 provide three time frames of protection. For times greater than 100 μs, the voltage across Q1 is prevented from exceeding the bus voltage by CR55-1, CR55-2, and CR54-2. The voltage across Q2 is prevented from exceeding the bus voltage by CR55-1, CR54-1, and CR55-2. Q3 and Q4 are similarly protected. In the intermediate time frame of 5 μs to 100 μs, C3 and C4 provide a low impedance ac clamp for the above diodes to work against. For the time frame of less than 5 μs, the voltage across a D7ST is clamped to the voltage of its associated C98-X by way of CR33-X. C98-X charges to nominally the bus voltage and is maintained at that voltage. As the time frame decreases, the associated protection components are mounted physically closer to the D7STs in order to minimize stray inductance. This combination of techniques keeps the voltage spikes across the D7STs to less than 50 V above the bus voltage and less than 1 μs in width, with peak currents greater than 300 A in the bridge and tank circuitry.

3.1.3 "Tailing" of the Collector Current

Initial testing of the converter revealed that the current in the transistor switches of Figure 6 was "tailing" out rather than following the half-sinusoidal shape of the tank current. This effect is shown in Figure 8 which depicts the ideal and "tailed" out waveforms. This "tailing" is due to stray inductance and the saturated inductance of the saturable reactors. For purposes of examination, Q2, CR2, CR54-2, T3-2, and SR1 of Figure 6 will be referenced specifically, but the following discussion applies to any of the four transistor switches. Also assume for the moment that T5 does not exist.

If Q2 is conducting, then when the half-sinusoidal current pulse passes 90°, the stray and SR1 inductances start to force the cathode of CR2 negative with respect to the bus return. As soon as the cathode of CR2 is ≈ 0.7 V negative, CR2 starts to conduct, with current circulating through CR2, SR1, T3-2, Q2, and back to CR2. The amount of inductance required to cause this problem can be calculated from

$$V = L \frac{di}{dt} \quad . \qquad (16)$$

The current in Q2 is $I = 200 \sin \omega t$ and $\omega = 1.26 \times 10^5$. Substituting into (16): $V = 200 \omega L \cos \omega t$. The maximum voltage developed will be $V_m = 200 \omega L$. If we assume that the total voltage drop across Q2, T3-2, and CR2 is 2 V, then $L = 7.9 \times 10^{-8} = 0.079$ μH. Therefore, a total inductance of 0.08 μH due to stray inductance and SR1 will begin to cause "tailing" in this circuit. It is not possible to keep even the stray inductance below 0.08 μH, and therefore a circuit change was required to eliminate the "tailing". The "tailing" cannot be tolerated because it causes turn-off losses in Q2.

Many schemes (> 20) were analyzed and/or evaluated in the circuit in an effort to solve this problem. This included the method used by Stuart[6] (at the University of Toledo) and others of putting inductance in series with each switch instead of using the saturable reactor of Figure 6. These techniques cannot be scaled to this power level and still keep the collector-to-emitter voltage on the transistor switches under control. Even if some of these techniques could have been scaled, they would only have eliminated the problem with the saturated inductance of the saturable reactors, and not the stray inductance problem.

The only scheme we found that works is the addition of transformer T5 of Figure 6. A portion of the voltage across the series-resonant inductor (L1) is fed back out-of-phase with the voltage developed across the stray and SR1 inductances and effectively cancels it out. The cathode of CR2 is not driven negative now; therefore, CR2 does not conduct, and the "tailing" is eliminated. The power removed from L1 by T5 is purely reactive and therefore does not introduce an efficiency penalty into the circuit (except for the small winding and core losses of T5).

3.1.4 Series Resonant Tank Components

The series resonant capacitor (C1) is made up of fourteen 0.25-μF ± 10% polypropylene capacitors in

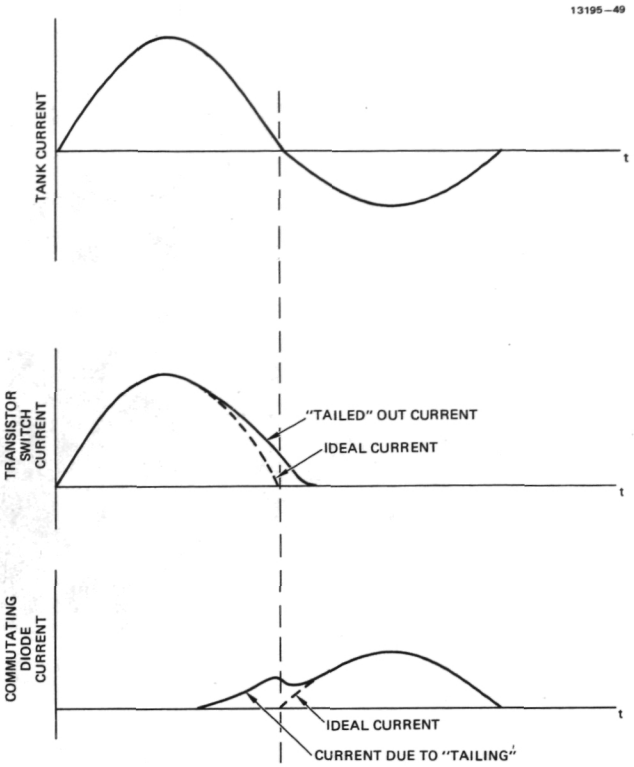

Figure 8. "Tailing" of the transistor switch current due to stray inductance.

parallel. Each capacitor is rated for 2000 Vdc and 25 A rms at 20 kHz. This particular capacitor was selected because of its ready availability from Component Research; it also provides a means of easily changing the total capacitance value in relatively small steps, which is desirable in a development program. Polypropylene is the only dielectric that is feasible at the required current and frequency because of its low dissipation factor.

The magnetic core configuration chosen for L1 and T1 is shown in Figure 9. The E-core configuration was chosen (over a C-core configuration) to minimize the air-gap fringe-flux interaction with surrounding components and structure. Each core is composed of six separate parts: two side bars, two end bars, and a two-section center post. The two-section center post allows the air gap to be placed in the center of this post, and the air gap can be adjusted by substituting various length center posts and/or moving the end bars in or out.

Mn60L ferrite from Ceramic Magnetics Inc. was chosen as the core material because of its very-low-loss characteristics (8 mW/cm^3) at 20 kHz and 1000 gauss; 45 mW/cm^3 at 20 kHz and 2000 gauss). The cores were sized to operate at 1000 to 1500 gauss where the losses will be less than 20 mW/cm^3. For the core shown in Figure 9, the total loss is less than 24 W, and therefore cooling of the core is not a problem. At full-power operation the temperature of the cores was below 40°C.

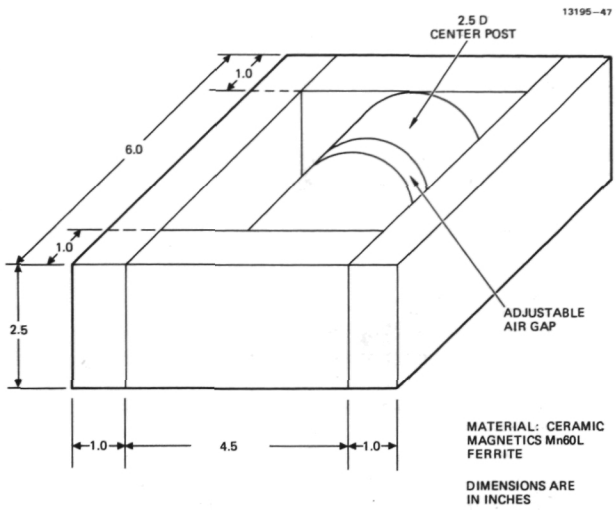

Figure 9. Core configuration for the resonant inductor and output transformer.

The series resonant inductor (L1) is wound with eight turns of 1323/36 (5 AWG) Litz wire on the center post of the ferrite E-core described above. The core has a 2.44-cm (0.96-in.) air gap in the center post. The secondary winding that feeds T5 is wound with ten turns of 150/36 Litz wire and is wound between the turns of the main winding. The output transformer has a 10-turn primary of 1323/36 (5AWG) Litz wire and two 22-turn secondaries of 210/33 (10 AWG) Litz wire wound on the center post of the ferrite E-core described above. The core has a 0.019-cm (0.0075 -in.) air gap in the center post, and the primary winding is sandwiched between the two secondary windings to improve coupling. The transformer has a primary leakage inductance of 1.9 μH and a primary inductance of 1.06 mH.

3.1.5. Output Transformer Saturation

When the converter is operating into a light load (~ 200 Ω), sub-resonant-frequency currents (that have also been observed by TRW[1] and Stuart[6] of the University of Toledo) flow in the series resonant tank. These sub-resonant-frequency currents result when the voltage on the resonant capacitor is still greater than the input bus voltage after the normal commutating diode-conduction period, and the modulation frequency is such that the tank current is discontinuous. Under these conditions, the commutating diodes start to conduct again in an effort to further lower the voltage on the resonant capacitor. The voltage applied to the output transformer is not sufficient to cause the output rectifiers to conduct, and therefore the primary inductance of the output transformer appears as part of the series resonant tank. The tank then starts to ring at a frequency determined by the resonant capacitor, the resonant inductor, and the output-transformer primary inductance (note that this is not a sub harmonic of the normal resonant frequency, but a function

of the output transformer primary inductance). These sub-resonant-frequency currents cause additional volt-seconds to be applied to the output transformer core with the result that the output transformer then approaches saturation during the normal resonant-frequency pulse. As the output transformer approaches saturation, it draws a very large magnetizing current (> 50 A). When the magnetizing current is equal to the resonant tank current, there is no current available for the output; therefore, the output rectifiers stop conducting and the primary inductance of the transformer is added in series with the resonant tank.

Figure 10(a) shows sub-resonant-frequency currents starting to flow approximately 85 μs after the start of the normal resonant current pulse and Figure 10(b) shows the effect of the output transformer approaching saturation. The T1 secondary current goes to zero before the tank current does (at ≈ 23 μs), which causes the T1 primary inductance to be inserted into the resonant circuit. The tank then starts to resonate at a lower frequency, followed by turn-off of the transistor switches at ≈ 28 μs.

This phenomenon does not cause any major problems in the operation of the converter or cause any components to be overstressed (with the possible exception of the transistor switches if they are not properly protected - see Section 3.4 below on protection circuits). It does cause jitter in the feedback loops and an increase in audio noise.

3.2 BASE DRIVE CIRCUIT

The base-drive strategy and basic circuit for driving the transistor switches was developed under Contract NAS3-22471 (Resonant Circuit Transistor Characterization).[2] The strategy developed is as follows. Regenerative (or proportional) feedback of the collector current is used since it minimizes the required power from the rest of the base-drive circuitry. At the same time, the transistor is maintained at a constant β (except during the leading-edge pulse), which saves on base-drive power. The base current is allowed to go to zero as the collector current goes to zero, which minimizes the storage time. The base-drive parameters from the transistor characterization that resulted in minimum total device dissipation are employed, and the base-emitter junction is kept reverse biased during the transistor off-time, which eliminates dV/dt turn-on caused by C_{OB} of the transistor switch.

Data taken on the D7ST transistor during Contract NAS3-22471 at 20 kHz and 250 A showed that a regenerative feedback ratio of 7:1, with a leading-edge pulse of 40-A amplitude and 12.5-μs width is required to keep the D7ST in saturation. It is also important that the leading-edge pulse have a rise time of 1 μs or less in order to minimize the turn-on time and get the transistor into saturation quickly. The turn-off pulse (negative I_B pulse) needs to be large in amplitude in order to minimize the storage time, which then allows for maximum utilization of the series-resonant tank.

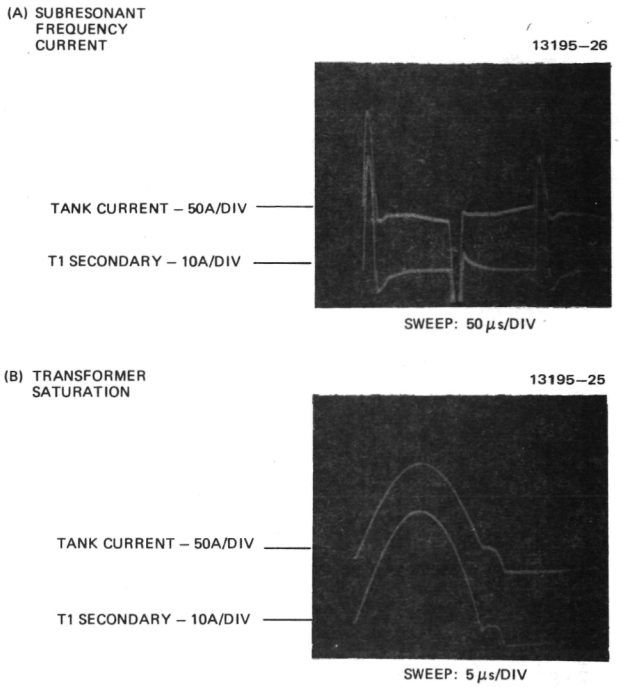

Figure 10. Sub-resonant-frequency currents and transformer saturation under light load (200 Ω) conditions.

Conventional transformer-coupled base-drive circuits will not provide a 40-A pulse with a rise time of 1 μs or less because of the leakage inductance of the transformer, base-emitter inductance of the transistor switch, and stray inductance of the wiring. The basic circuit of Figure 11 was developed under Contract NAS3-22471 to provide a 40-A pulse with a rise time of 1 μs or less and a 7:1 regenerative feedback ratio. Referring to Figure 11, CR30 and L2 resonantly charge capacitor C6 to approximately 70 V. When Q6 is turned on to apply a leading-edge pulse to Q1, the high voltage charge on C6 is applied to the primary of T4. This high voltage overcomes the effect of the leakage inductance of T4, the stray wiring inductance, and the base-emitter inductance of Q1, allowing the base current to rise to 40 A in approximately 1 μs. After the charge on C6 has decayed to 15 V the remainder of the leading-edge pulse is supplied from the 15-V source through CR5. The width of the leading edge pulse is controlled by the on-time of Q6.

The regenerative feedback is supplied by transformer T3. A separate transformer is used for the regenerative feedback so that the leakage inductance of T4 (supplying the leading-edge pulse) can be minimized. Transistors Q7, Q8, and Q10 are used to isolate the transformers so that the base of Q1 can be held at a negative bias during the

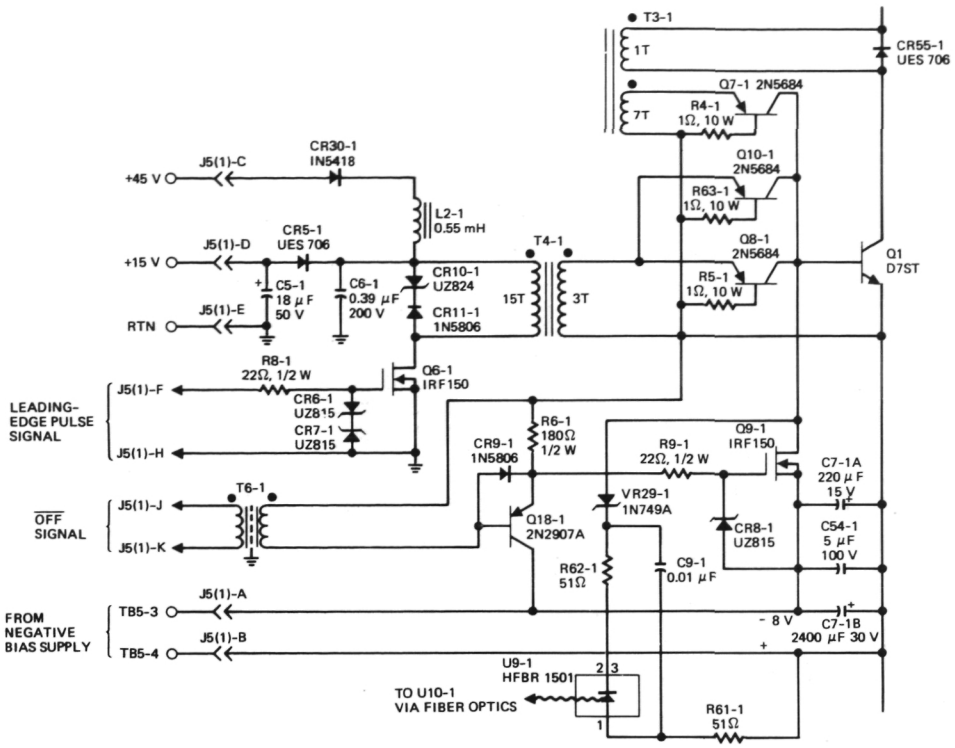

Figure 11. Base-drive circuitry for the 25-kW converter (one of four).

time that it is turned off. Q9 supplies the turn-off pulse to the base of Q1 and holds it at the negative bias level of -8 V.

A base-emitter voltage-sense circuit composed of VR29, R61, R62, C9, and U9 was added to provide an indication of whether the D7ST is ON or OFF. If the base-emitter voltage is greater than -5V the D7ST is considered to be ON, if this voltage is less than -5V it is considered to be OFF. A value of -5V was chosen as the transition point since during turn-off, the base-emitter voltage that can be measured (terminals on the transistor package) is a few volts negative while the transistor itself is still forward biased. This is due to the resistance and inductance that exists inside the transistor package.

Standard optical couplers, such as a 6N136, were found to be inadequate for use in this base-emitter voltage-sense circuit (U9-U10 combination). The input-to-output capacitance of these devices (~ 1 pF for a 6N136) is sufficient to cause false signals under the 1000-V/μs conditions that exist in the circuit. Replacing the optical coupler with a fiber-optic link was the only way found to eliminate the noise problem and still maintain the sub-microsecond response required of the circuit.

Figure 12 shows the transistor switch (D7ST) base-drive waveforms provided by the circuit of Figure 11. The leading-edge pulse is 50 A in amplitude and 12.5-μs wide. The turn-off pulse is -30 A, which keeps the storage time down to ~ 4 μs. Initial testing of the converter was done with a 40-A leading-edge pulse which resulted in a power stage efficiency of 92% at 25 kW and 350 V input. Increasing the leading-edge pulse to 50 A increased this efficiency to 94.3% at the cost of only 80 W of housekeeping power. This represents an overall efficiency gain of 2% and demonstrates the necessity of getting the transistor switches into hard saturation quickly.

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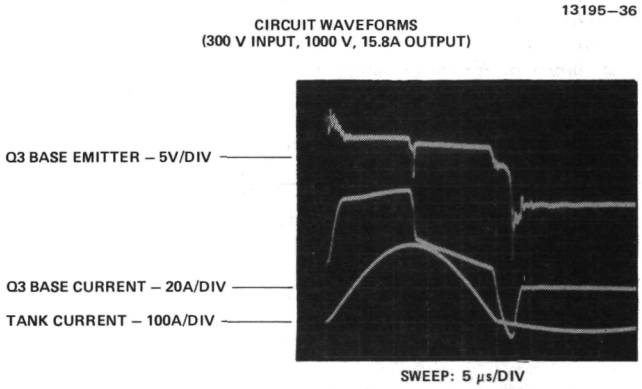

Figure 12. Transistor switch (D7ST) base-drive waveforms.

3.3 *OUTPUT CIRCUITRY*

The schematic of the output circuitry is shown in Figure 13. The ac current supplied by T1 is rectified by two full-bridge circuits, CR12 through CR15, and CR16 through CR19. The split secondary

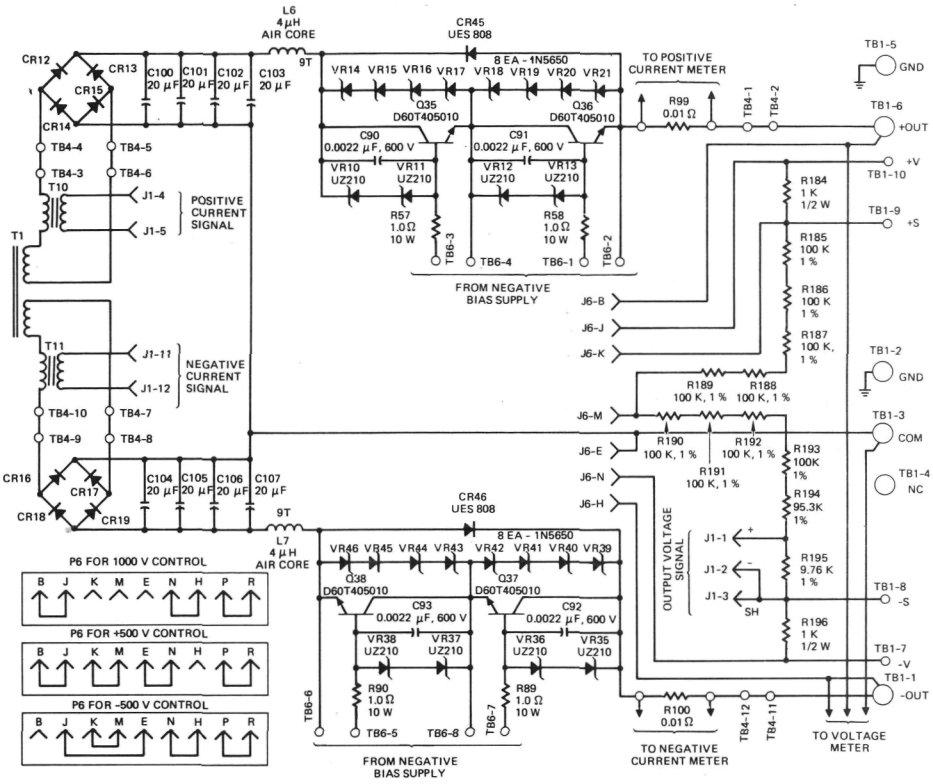

Figure 13. Output circuitry of the 25-kW converter.

on T1 and the two recitifier circuits allow the output to be configured as a single 0-to-1000-V output or as a dual 0 to ± 500 V output. The two halves of the output are filtered by C100 through C103 and C104 through C107. The filtered power is then connected to the output terminals through transient-output-current limiters (Q35/Q36 and Q37/Q38 with their associated components). Only the positive output current limiter will be discussed since the negative output operates in an identical manner. Q35 of Figure 13 receives a constant base-drive current, and therefore acts as a constant-current source (beta times its base current). The base drive is set for a constant collector current of ~ 60 A, which keeps Q35 in hard saturation over the normal output-current range of 0 to 30 A. When a transient-current condition exists (> 60 A), Q35 comes out of saturation and limits the current to 60 A. In practice, a relatively large current spike (~ 250 A) exists on the leading edge of a transient, as shown in Figure 14. This current spike is due to the excess carriers stored in Q35. Once the excess carriers are depleted, Q35 tries to come out of saturation very quickly (< 100 ns). If allowed to do so, a destructive voltage transient would result on the collector of Q35 due to high di/dt and circuit inductance. To prevent this destructive voltage spike from occuring, C90, VR10, and VR11 were added to the circuit to limit di/dt to a safe value. VR14 through VR17 are transient voltage suppressors that limit the voltage across Q35 to ~ 250 V and force it to share the voltage with the other transistors (Q36, Q37, and Q38). Inductor L6 was added to the

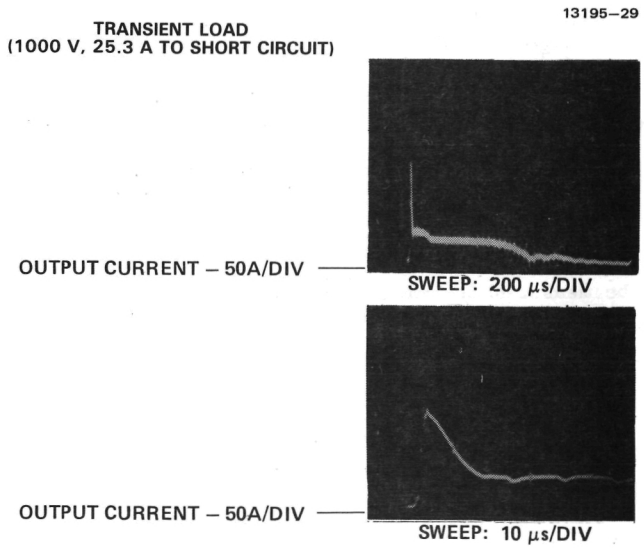

Figure 14. Transient output current during a transient from full load to short circuit.

circuit to roll off the leading-edge on very fast transients. Figure 14 shows the large current spike on the leading edge which lasts for ~ 25 μs, then a current plateau at 75 A for ~ 150 μs which corresponds to current flowing through the transient voltage suppressors as well as the transistors, another plateau at 60 A lasting ≈

600 μs and representing the beta-limited current of the transistors, and finally the current falling to 25 A as the stored charge in the output capacitors is depleted.

3.4 CONTROL AND PROTECTION CIRCUITS

The control circuitry for the converter involves four feedback loops: one for controlling the output voltage, one for controlling the average current in the tank circuit, one for controlling the current in the positive-output leg, and one for controlling the current in the negative-output leg. All four loops have separate reference signals and automatically crossover from one loop to another, with each loop preventing its controlled parameter from exceeding the value set by its reference signal. Protection circuits are included to prevent the output voltage from exceeding 50 V over the reference level, to prevent the peak tank current from exceeding 350 A, to prevent the transistor switches from turning off if the tank current is greater than 70 A, and to trip the input circuit breaker if the bus voltage falls below 50 V, if Q1 and Q2 or Q3 and Q4 are on simultaneously, or if the Q1 or Q4 collector currents flow for greater than 50 μs. The control and protection circuitry are shown in Figure 15.

The output voltage feedback-signal is isolated from the floating output by isolation amplifier AR1. This feedback signal is then compared against the output-voltage-reference signal (V_{REF}) and the difference integrated by AR2. AR2 also provides a lead-lag network for loop compensation. Comparator U16 senses when the output voltage is more than 50 V higher than the referenced level and immediately triggers the integrator reset circuit. This keeps the output voltage under control during transient and open circuit conditions.

The sum of the average current in the positive-output leg and the negative-output leg is related to the average current in the series-resonant-tank circuit by the turns ratio of T1. Therefore, the average tank current can be sensed and used to control the sum of the output currents, while at the same time protecting the bridge and tank-circuit components. The tank current is sensed by current transformer T2, rectified, and converted to a voltage by R34. This voltage is then compared against the tank-current reference signal ($I_{TANK\ REF}$) and the difference integrated by AR3. AR5 senses when the output voltage has fallen below a certain level (determined by the tank current reference-signal - 185 V for a reference level of 25 A) and then linearly phases the output current back to 11 A as the output voltage falls to zero. Comparator U15 senses when the peak tank current exceeds 300 A and immediately triggers the integrator-reset circuit, which in turn phases the inverter OFF. The integrators can immediately start to integrate and phase the inverter back ON to the referenced set point. This comparator limits the peak tank current and protects the components of the bridge and tank circuitry during transient conditions. Currents are limited to a peak value of 350 A and the voltage on resonant capacitor C1 is limited to 1600 V.

The outputs from the voltage and current feedback circuits, along with the integrator reset signal, are diode-OR'd to the input of the V/F converter. The output pulses from the V/F converter provide the basic repetition rate at which the transistor switches in the bridge circuit are turned ON and OFF. The pulses from the V/F converter are AND'd, with the reverse base-bias signals by U11. This guarantees that all four transistor switches are OFF before trying to turn any of them ON. In reality, this prevents turning Q1 and Q3 ON while Q2 and Q4 are ON, and vice-versa. The output of U11 is alternately switched between X and Y by the steering gates. This 22-μs-wide pulse sets the ON time of the transistor switches before the turn-off pulse is applied. Due to storage time the transistor switches do not actually turn-off until they have been ON for 25 μs, which is the period of a half-sinusoidal resonant-current pulse. The outputs of the steering gates are OR'd with the output of U27 which is triggered if Q1 and Q2 or Q3 and Q4 are ON simultaneously. When U27 is triggered, all four bridge transistors are turned ON for 400 μs. The reason for doing this will be discussed later in this section.

The U4 output pulses follow two paths. First, they are applied to U26 which effectively turns Q9 of the base-drive circuits OFF, permitting QX of the bridge circuit to be turned ON. The trailing edge of the pulse from U4 turns Q9 back ON, starting the turn-off of QX unless prevented from doing so by the gating logic from U28 and U29. This gating logic prevents turning QX OFF until the tank current is below a level at which it is safe to do so (input from U28 and U29). The gating logic blanks the pulses from U28 and U29 that are associated with commutating diode conduction.

The output pulses from U4 are also delayed for approximately 1 μs. This delay allows time for Q9 to turn OFF and also provides a means of balancing both halves of the tank current, if necessary, by varying this time delay slightly. The delayed pulse is then shortened by U5 to the width required for the leading-edge base-drive pulse (≈ 12 μs). This shortened pulse is then used to drive Q6-X of the base-drive circuitry.

The tank-current level detection circuitry consists of comparators U28 and U29 (one for positive tank current and one for negative tank current) which compare the tank current against a fixed reference. The outputs from these comparators prevent the base-drive logic from turning-off the D7ST transistors in the tank circuit until their collector currents are below a safe level. The safe level is determined by the reverse-biased safe-operating area (SOA) of the D7ST transistors. However, reverse-biased SOA curves are not available for the D7ST and

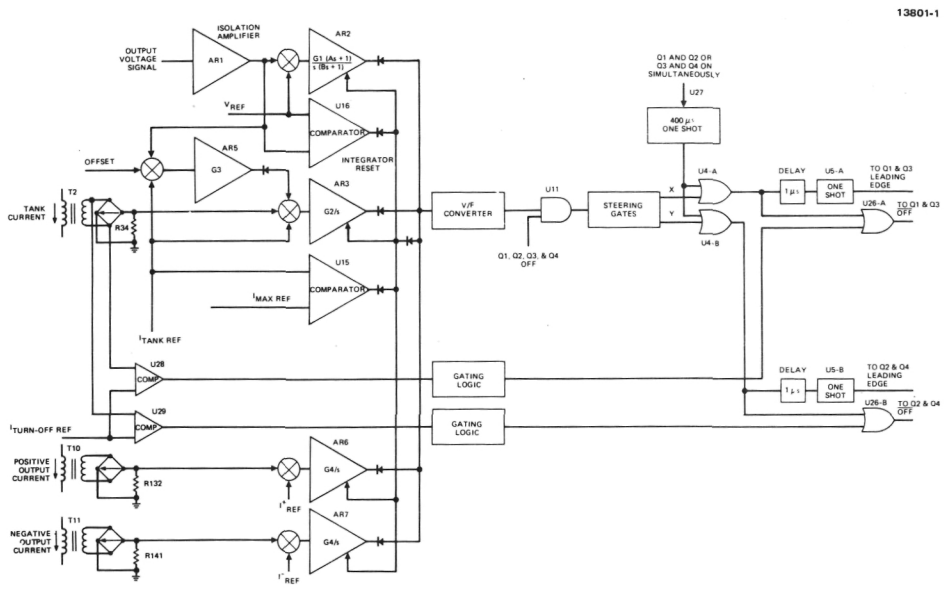

Figure 15. Control and protection circuitry.

therefore this circuit was set by empirical data at 70 A. No failures of the D7STs occurred at this value, but one failure did occur at 90 A.

The protection philosophy for the D7ST switches that was embodied in the original design of this converter (and also the 10-kW converter developed under contract No. NAS 3- 22471) was to turn all four of them OFF in the event of a malfunction. However, transistors in general can absorb much more energy (> 10 times) if they are forward biased than if they are reverse biased. Therefore, a better approach to protecting them during a malfunction is to turn them ON. Turning all four bridge transistors ON places a short on the input bus, and therefore the input circuit breaker must be opened quickly in order to isolate the input bus from the short. The input circuit breaker opens in less than 20 μs and the input filter provides the isolation during this time. U27 of Figure 15 turns all four bridge transistors ON if the reverse-base-bias circuitry senses that Q1 and Q2 and/or Q3 and Q4 are on simultaneously. The steering gate logic guarantees that the control circuitry does not try to turn the D7STs OFF before the end of the normal resonant half-cycle, and the tank-current level detectors guarantee that the D7STs are within their reverse-biased safe-operting-area before they are turned OFF. No D7ST failures occurred after all of this circuitry was incorporated.

3.5 INPUT BUS PROTECTION

The main dc bus for the inverter is protected by a solid-state circuit breaker. The switch used in this circuit breaker is a D7ST transistor that is driven by a small, free-running inverter operating at 50 kHz. The circuit breaker is opened and closed by turning the inverter circuit OFF and ON. During opening of the circuit breaker, an SCR is also triggered, which draws 70 A of reverse base current from the D7ST. This reduces the opening time to 12 μs. Without the SCR, it takes 100 μs for the circuit breaker to open. The circuit breaker is followed by a two-stage LC filter with an attenuation of 99% at 20 kHz.

3.6 MECHANICAL

The 25-kW converter was designed to be used in a laboratory type environment with forced air as the cooling medium. It is self contained in a rack-mountable chassis that is 48.25-cm W x 62.25-cm H x 61-cm D (19-in. x 24.5-in. x 24-in.) and weights 135.6 kg (299 lb). The components of the 25-kW converter weigh 54.28 kg. This weight includes harness, printed circuit cards and mounting hardware, but does not include heatsinks, blowers, front panel components, or unregulated-power components. The specific weight of the components is 2.17 kg/kW and the specific weight of the converter as delivered is 5.42 kg/kW. For a flight-type packaging design, with a packaging factor of 1.7 to 2.0, the converter should have a specific weight in the range of 3.7 to 4.3 kg/kW.

4. TESTING

The 25-kW converter that was designed, developed, and fabricated under this contract was also tested under a variety of conditions to determine its operational characteristics. Testing was conducted for stability, steady-state waveforms, output ripple, input current ripple, regulation, transient waveforms, and efficiency. The major test results are discussed in the following paragraphs.

The voltage and the current control loops all have integrators in their forward loops to provide

very high dc gain, necessary for good regulation. In addition to the integrator, the voltage-control loop has a lead-lag network on the input of its integrator for loop compensation. The bandwidth of this loop increases and the stability decreases as either the output voltage increases or the load resistance decreases. The worst-case gain margin is 10 dB, and the worst-case phase margin is 45°.

The current control loops do not have any compensation in addition to their integrators. The bandwidth and the stability of these loops are similar to the voltage loop for the conditions tested, with a worst-case gain margin of 6 dB and a worst-case phase margin of 65°. The positive output current loop and the negative output current loop are identical to the tank current loop except that they are 4-dB lower in gain.

Photographs of oscilloscope traces of the major current and voltage waveforms in the inverter were taken for various output conditions. Figure 16 shows the Q3 base-drive current, resonant capacitor voltage, and tank current for a 300-V input, a 40-Ω load, and output voltages of 200, 600, and 1000 V. At an output of 1000 V and 25.3 A the peak tank current is 240 A and the peak voltage on the resonant capacitor is 700 V.

The input bus voltage and current are shown in Figure 17 during turn-on to a full load output. Figure 17(a) shows turn-on of the power stage with the input circuit breaker already closed. The input current is well behaved and does not overshoot. The little blip at 3 ms is associated with the automatic crossover between one control loop and another which occurred at that time. Figure 17(b) shows closing of the input circuit breaker with the power stage already ON. There is a 330-A current spike which decays to zero in 700 μs, and then the current starts to rise again in a controlled manner. The large current spike is the result of charging up the input filter and is not associated with converter operation.

The tank current, output current, and input current response to a load transient of 1000 V at 25.3 A to short circuit is shown in Figure 18. The tank current is limited to a peak of 300 A and the effect of the peak tank current limiting circuitry can be seen. The converter is phased completely OFF at 50 μs by way of the peak tank current limiting circuitry having reset all the integrators in the control loops. At 170 μs the integrators are phasing the converter back ON in a controlled manner. The output current is limited by the output-transient-current limiters as described above. The input current shows a slight increase in amplitude at 100 μs and then drops toward zero.

The response of the tank current, input current, and output voltage to a load transient of open circuit at 1000 V to a full load of 1000 V at 25.3 A is shown in Figure 19. The input current overshoots ~ 20 A for 1 ms as the converter recovers from the transient. The output voltage drops ~ 150 V as the full load is applied and recovers within 2 ms.

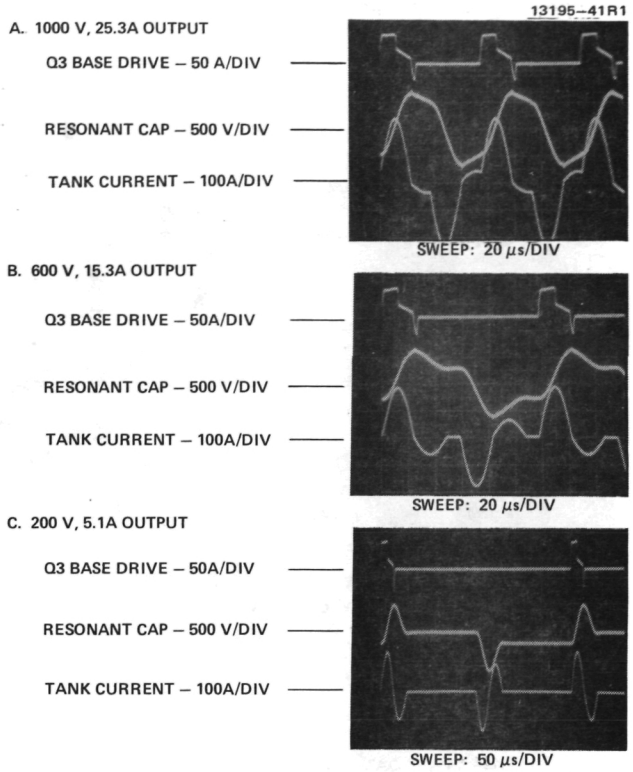

Figure 16. Steady-state base-drive, resonant-capacitor voltage, and tank current waveforms for a 40-Ω load and 300 V input.

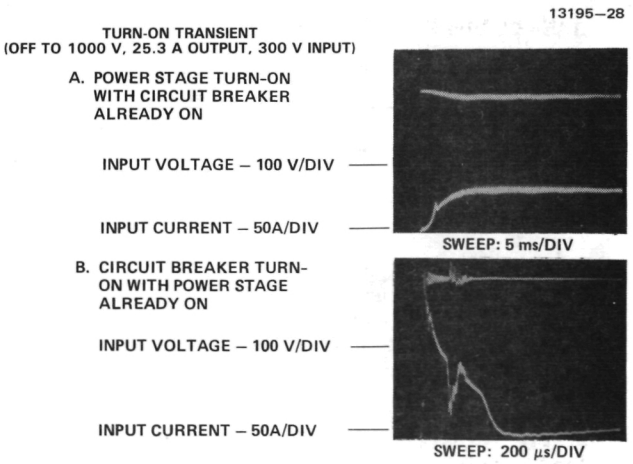

Figure 17. Input bus voltage and current during turn-on to the full load output.

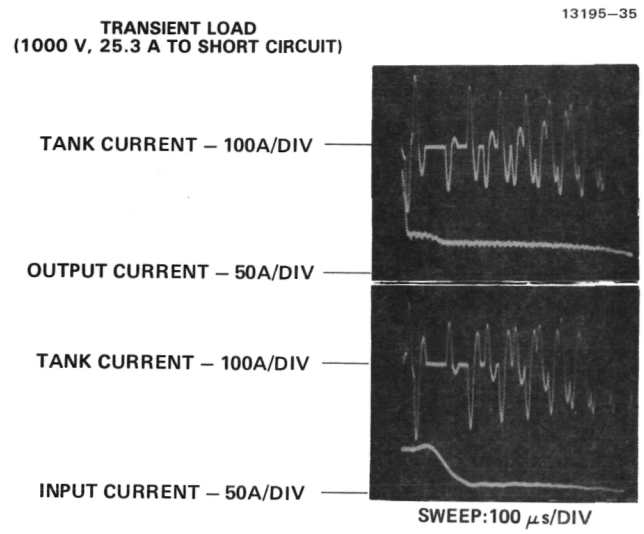

Figure 18. Tank current, output current, and input current response to a load transient of 1000 V at 25.3 A to short circuit.

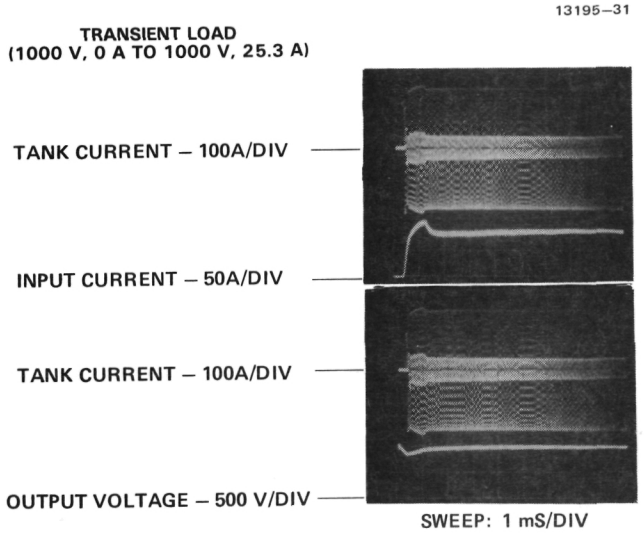

Figure 19. Tank-current, input-current, and output-voltage response to a load transient of open circuit at 1000 V to full load of 1000 V at 25.3 A.

The efficiency of the converter was measured under static conditions while operating into a resistive load. This coverter contains two elements that are not normally associated with the efficiency numbers quoted for converters: the input circuit breaker and the output-transient-current limiters. The total efficiency (including housekeeping power) curve versus output power is shown in Figure 20 for a constant output of 1000 V. The figure shows that the efficiency is nearly constant for output power levels above 6 kW. The converter was operated at 30 kW (1000 V, 30 A output) for inputs of 300 and 350 V. As can be seen from Figure 20, the efficiency drops off at 30 kW, due primarily to an increase in the saturation voltage of the D7STs at these power levels. The 300-V input, 1000-V/25-A output operating point has a total efficiency of 93.5%, housekeeping power accounts for 0.66%, and the input circuit breaker and output-transient-current limiters account for 0.54% of the difference in efficiency from the ideal of 100%.

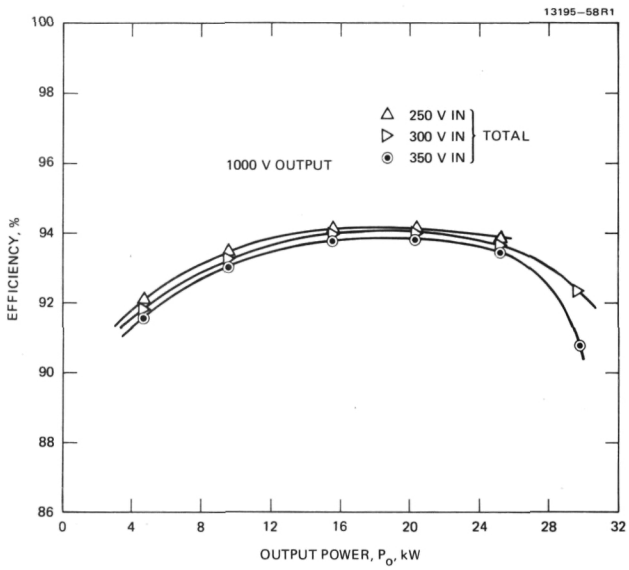

Figure 20. Total efficiency versus output power for a constant 1000-V output.

5. CONCLUSIONS

The feasibility of processing 25-kW of power with a single, transistorized, series resonant converter stage has been demonstrated by the successful design, development, fabrication, and testing of such a device. It employs four Westinghouse D7ST transistors in a full-bridge configuration and operates from a 250 to 350 V dc input bus. The unit has an overall worst-case efficiency of 93.5% at its full rated output of 1000 V and 25 A dc . A solid-state dc input circuit breaker and output-transient-current limiters are included in and integrated into the design.

There are no inherent problems that would prevent this 25-kW design from being upgraded to a space-qualified status. The major areas that would need to be addressed are:

- Reliability and qualification of the D7ST transistors.
- Electrical design with reduced core size and thermal design of the series resonant inductor and output transformer.
- Input filter design to meet MIL-STD-461B.
- A method of precharging the input filter to prevent large in-rush currents when the input circuit breaker is closed.
- Thermal-vacuum packaging of the entire unit, including heat pipes and the bridge circuit electrical layout, which is critical.

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